In the Specification:

Please amend paragraph **[0027]** as follows:

As shown in FIG. 2A, in a first alternative version, a bitline signal is input to the gate of an n-type conductivity field effect transistor (hereinafter, NFET) N2, in which the source is coupled to a fixed potential, for example ground, as shown in FIG. 2A, and the drain 112 is coupled to a sense amplifier 116 [[16]]. In FIG. 2A, NFET N2 and at least NFET N4 are transistors of an array of transistors including a storage cell transistor array of the memory. Thus, as will be described in more detail below, N2 and N4 are located within the same transistor array in which transistors of the storage cell array are located, and are fabricated in essentially the same manner as these transistors, as will be described with reference to the exemplary implementation in FIGS. 3A-3C below. Hereinafter, transistors which are labeled with an "N" preceding a number shall be understood to be NFETs. In this configuration where the source of the NFET is coupled to ground, the voltage appearing at the drain of N2 is inverted relative to the voltage applied to its gate. The voltage appearing at the drain 112 of N2 is also an amplified output of transistor N2 because a small change in the voltage applied to the gate of transistor N2, e.g. from a value just below the threshold voltage of N2 to a value above the threshold voltage, causes the voltage at the drain 112 to change from its prior level to ground, as the transistor changes to a conductive state.

Please amend paragraph **[0044]** as follows:

Still another version of the embodiment shown in FIG. 2A is provided in FIG. 2C. In this version, rather than using an arbitrary fixed reference voltage Vref to generate an output on line 132 for comparison by sense amplifier 136 with the voltage on line 130, the reference voltage is provided by a non-accessed bitline (/BL) of the storage cell array. The non-accessed ~~the non-accessed~~ bitline /BL acts as a reference bitline which is allowed to float at the time that the active bitline voltage BL is input to transistor N 14. The non-accessed bitline (/BL) can be an adjacent bitline of the same storage cell array as the bitline BL, when the storage cell array is a folded bitline array, as is bitline 17 described above relative to FIG. 1A. Such is a preferred arrangement for common mode noise rejection, since the non-accessed bitline /BL crosses the same space of the storage cell array, and is thus subject to the same sources of noise and interference as bitline BL. In a folded bitline array, depending on the wordline that is accessed, when a storage cell on a bitline BL is accessed, bitline /BL is non-accessed. Conversely, at other times, a storage cell on a bitline /BL is accessed, at which times the bitline BL becomes the non-accessed bitline.